FIG.1

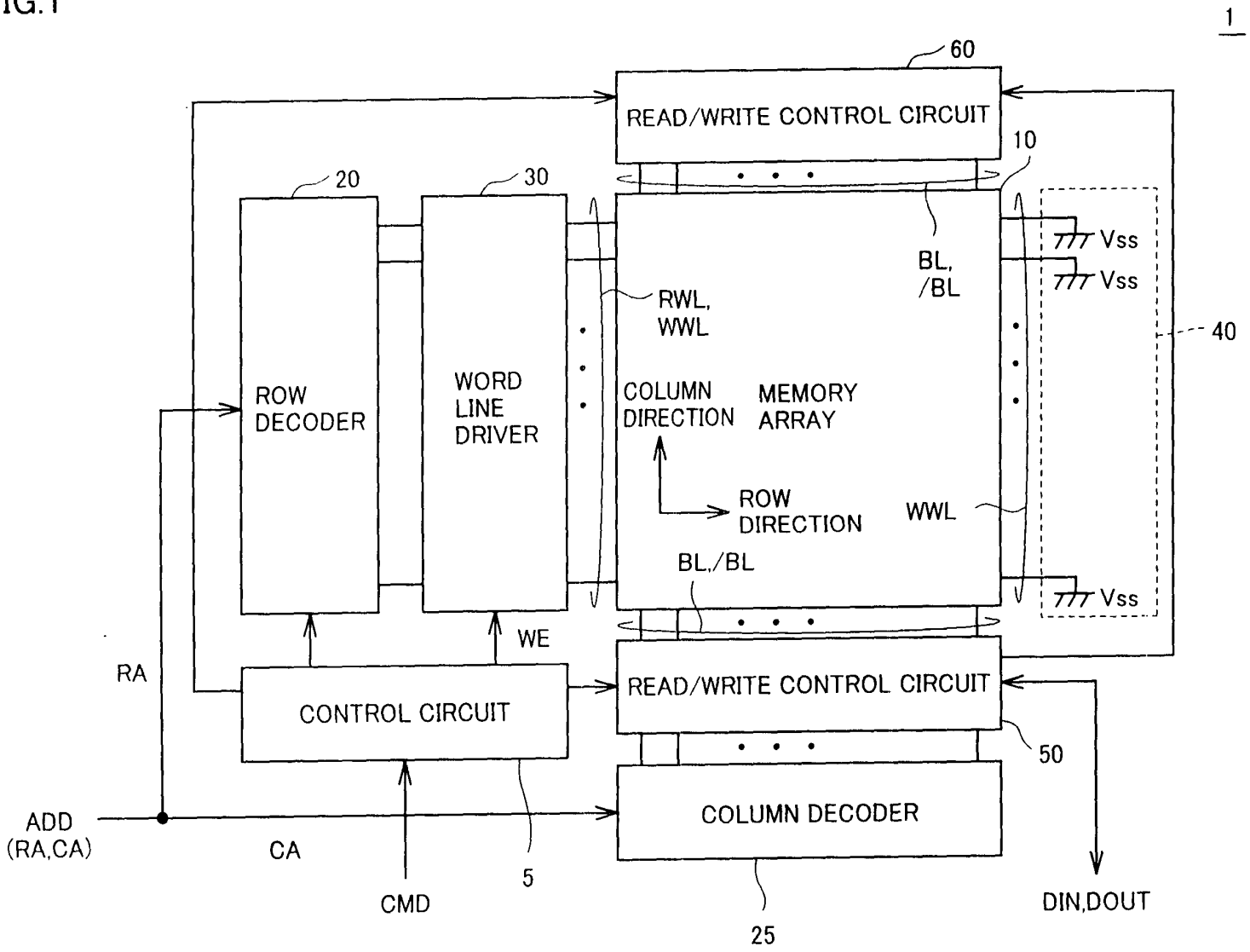
1
60
READ/WRITE CONTROL CIRCUIT
10
20
30
ROW DECODER
WORD LINE DRIVER
RWL, WWL
BL, /BL
Vss
Vss
40
COLUMN DIRECTION
MEMORY ARRAY
ROW DIRECTION
WWL
BL,/BL
Vss
WE
RA
CONTROL CIRCUIT
READ/WRITE CONTROL CIRCUIT
50
ADD (RA,CA)
CA
CMD
5
COLUMN DECODER
25
DIN,DOUT

FIG.2

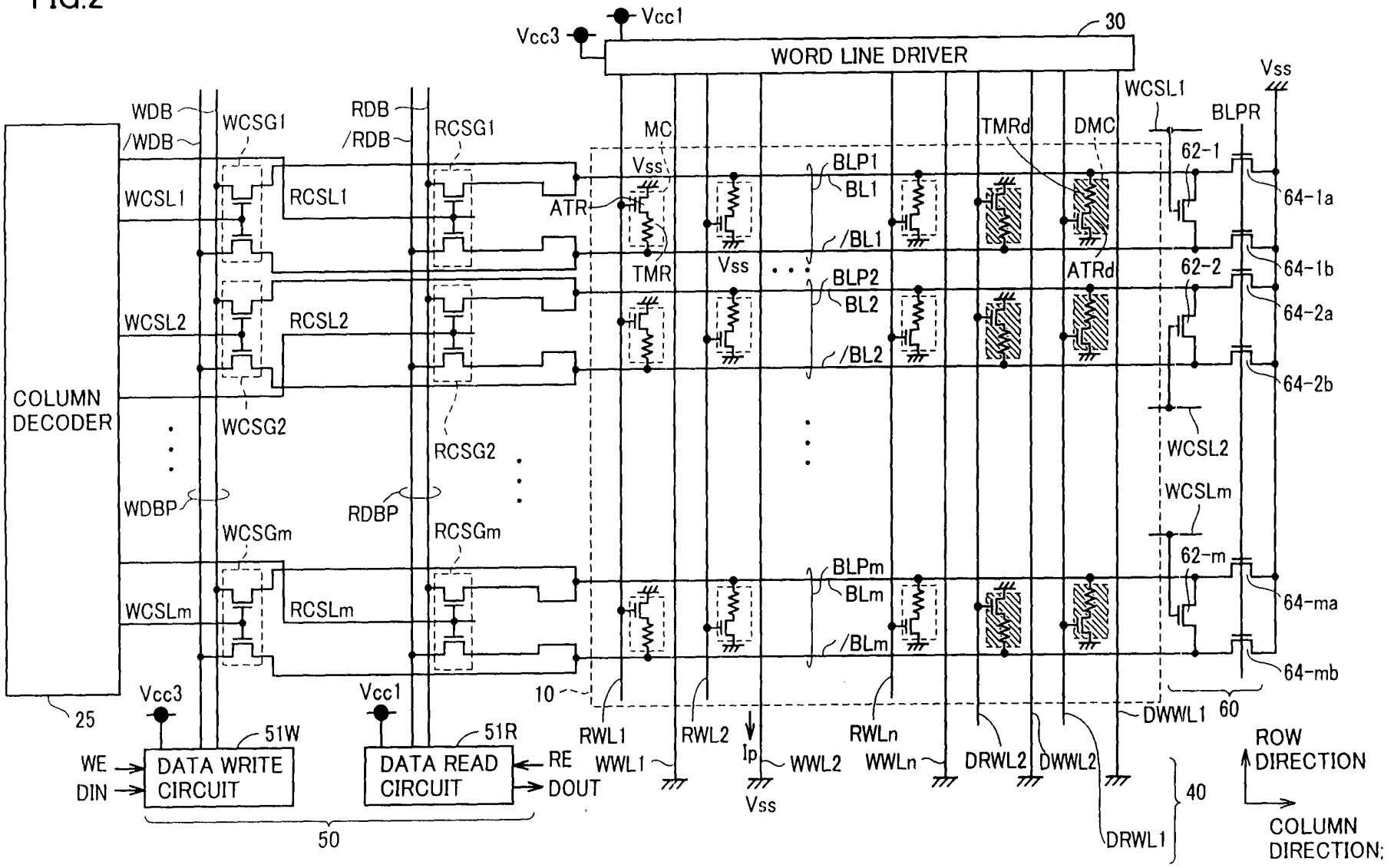
Vcc3
Vcc1
WORD LINE DRIVER
30
Vss
WDB
/WDB
WCSG1
RDB
/RDB
RCSG1
MC
TMRd
DMC
WCSL1
BLPR
62-1
64-1a
Vss
BLP1
BL1
/BL1
ATR
TMR
Vss
ATRd
62-2
64-1b
64-2a
BLP2
BL2
/BL2
64-2b
WCSL1
WCSL2
RCSL1
RCSL2
COLUMN DECODER
WCSG2
RCSG2
WCSL2
WCSLm
WDBP
RDBP
WCSGm
RCSGm
BLPm
BLm
/BLm
62-m
64-ma
64-mb
WCSLm
RCSLm
10
DWWL1
60
25
Vcc3
Vcc1
51W
51R
RWL1
RWL2
Ip
RWLn
DRWL2
DWWL2
ROW DIRECTION
WE
DIN
DATA WRITE CIRCUIT
DATA READ CIRCUIT
RE
DOUT
WWL1
WWL2
WWLn
DRWL1
40
COLUMN DIRECTION
Vss
50

FIG.3

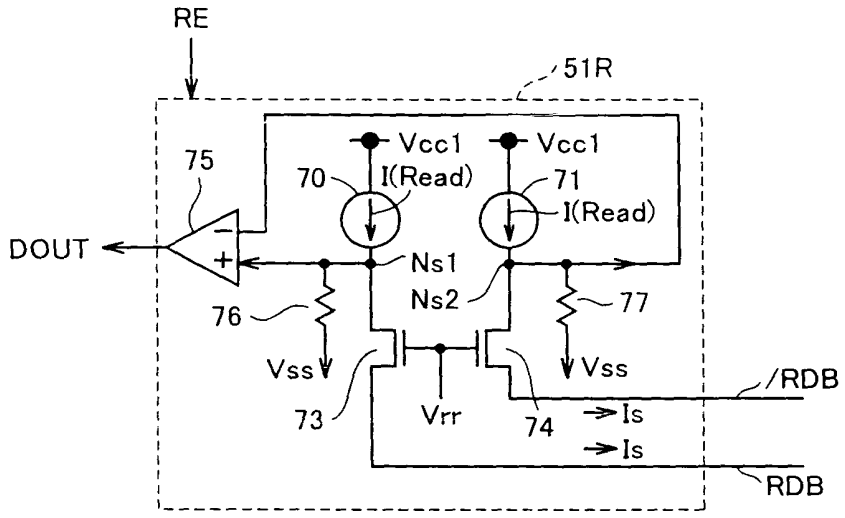
RE
51R
Vcc1
Vcc1
75
70
I(Read)
71
I(Read)
DOUT
Ns1
Ns2
76
77
Vss
Vss
/RDB
73
Vrr
74
Is
Is
RDB

FIG.4

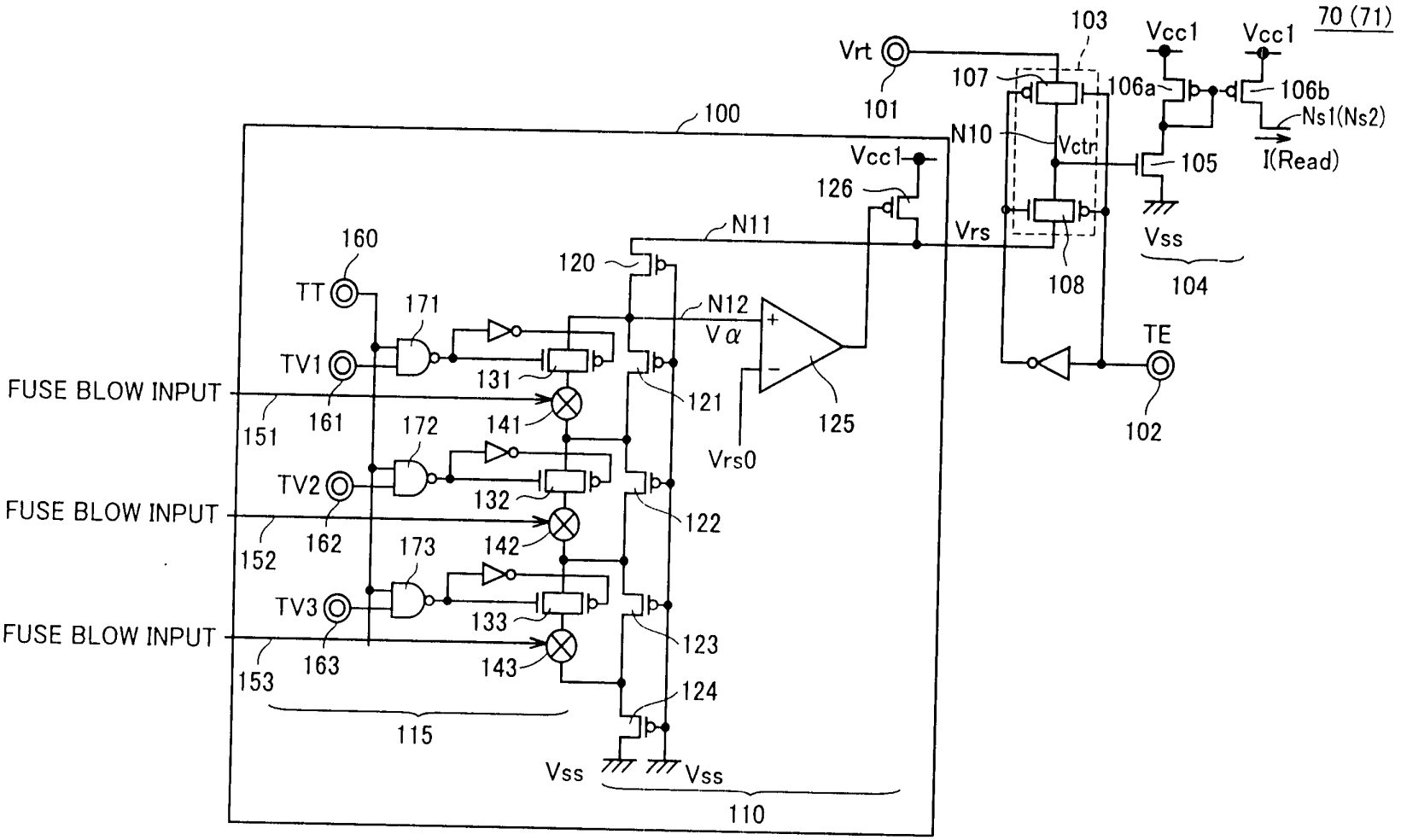
70 (71)
Vrt
101
103
Vcc1
Vcc1
107
106a
106b
Ns1(Ns2)
I(Read)
100
N10
Vctn
Vcc1
105
126
N11
Vrs
Vss
104
160
TT
171
120
N12
Vα
108
TE
TV1
131
121
125
FUSE BLOW INPUT
151
161
172
141
Vrs0
102
TV2
132
122
FUSE BLOW INPUT
152
162
173
142
TV3
133
123
FUSE BLOW INPUT
153
163
143
124
115
Vss
Vss
110

FIG.5

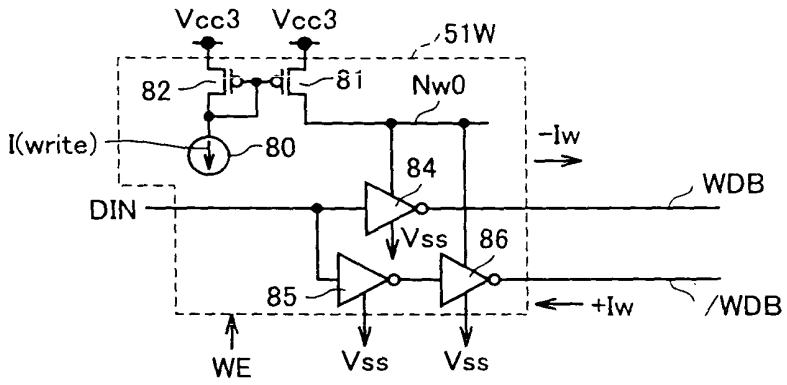
Vcc3
Vcc3
51W
82
81
Nw0
I(write)
80
-Iw
84
WDB
DIN
Vss
86
85
+Iw
/WDB
WE
Vss
Vss

FIG.6

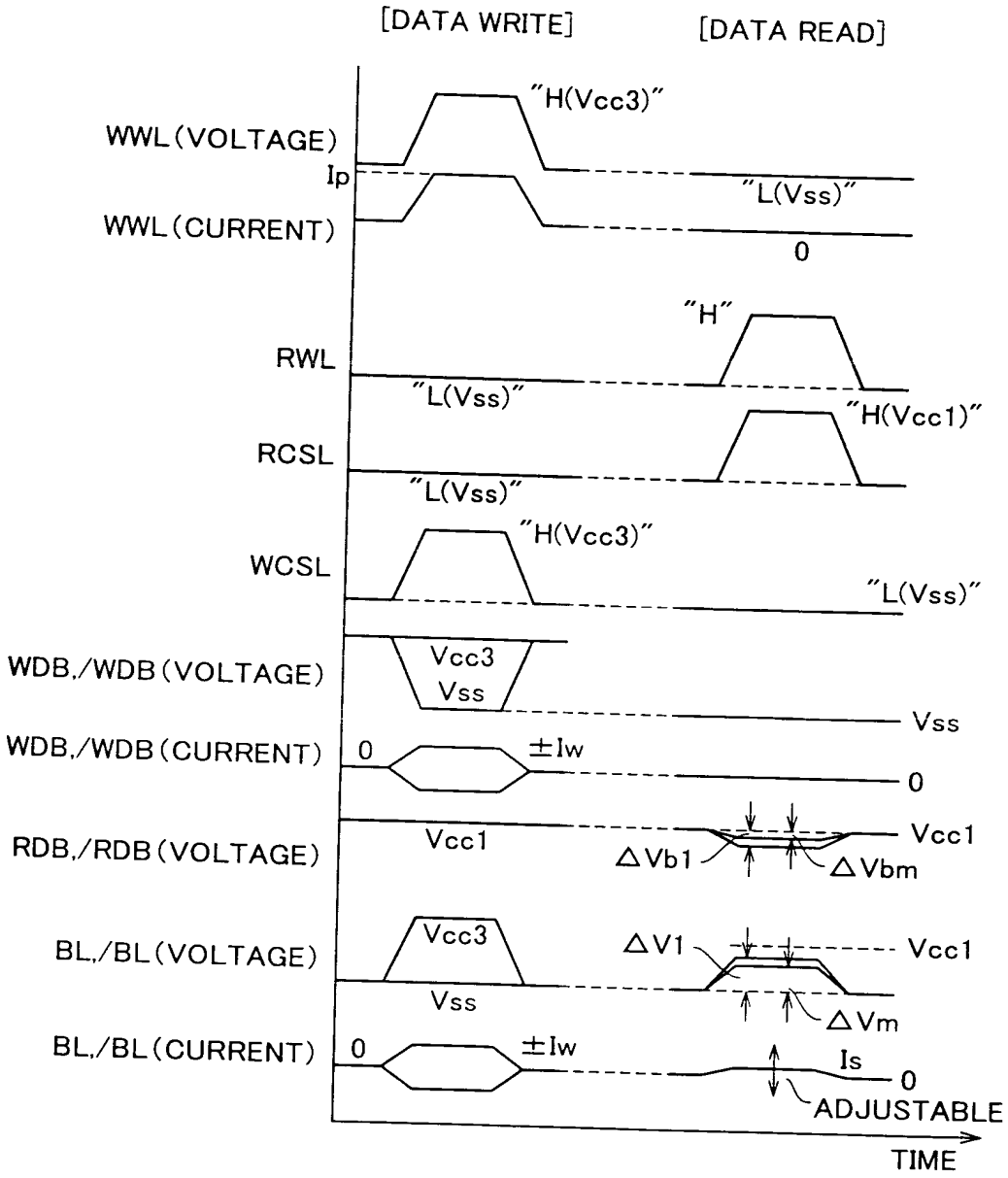
[DATA WRITE]
[DATA READ]
WWL(VOLTAGE)
"H(Vcc3)"
Ip
"L(Vss)"
WWL(CURRENT)
0
"H"
RWL
"L(Vss)"
"H(Vcc1)"
RCSL
"L(Vss)"
"H(Vcc3)"
WCSL
"L(Vss)"
WDB,/WDB(VOLTAGE)
Vcc3
Vss
Vss
WDB,/WDB(CURRENT)
0
±Iw
0
RDB,/RDB(VOLTAGE)
Vcc1
Vcc1
ΔVb1
ΔVbm
BL,/BL(VOLTAGE)
Vcc3
ΔV1
Vcc1
Vss
ΔVm
BL,/BL(CURRENT)
0
±Iw
Is
0
ADJUSTABLE
TIME

FIG.7

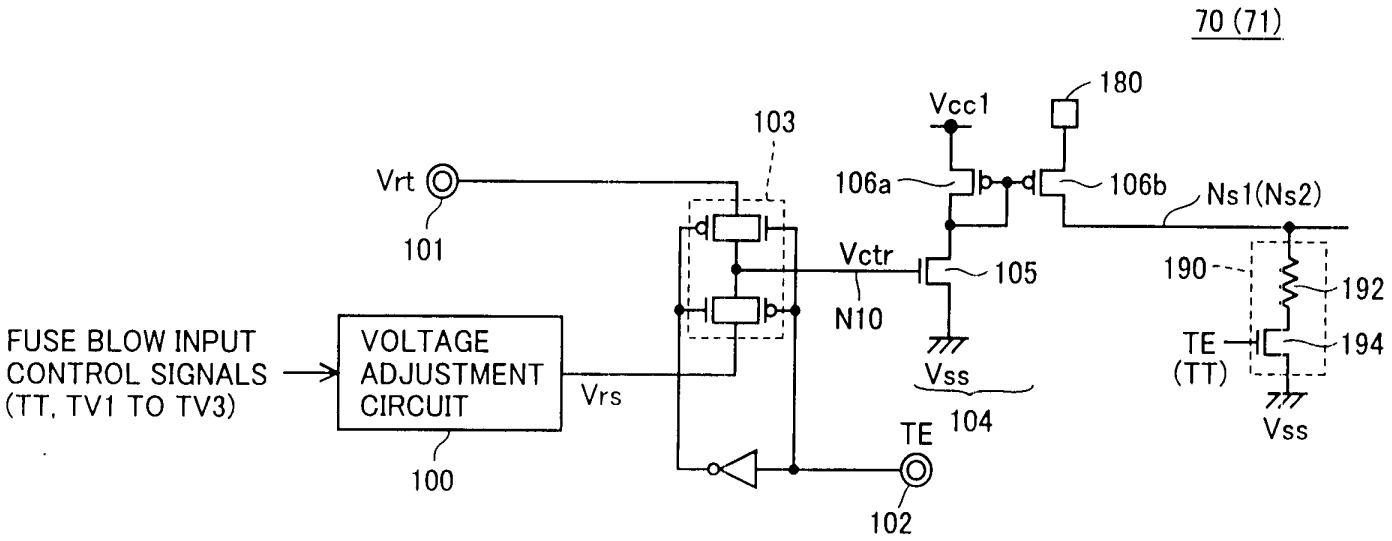
70 (71)
180
Vcc1
103
Vrt
101
106a
106b
Ns1(Ns2)
Vctr
105
190
192
N10
FUSE BLOW INPUT
CONTROL SIGNALS
(TT, TV1 TO TV3)
VOLTAGE
ADJUSTMENT
CIRCUIT
Vrs
Vss
104
TE
(TT)
194
TE
Vss
100
102

FIG.8

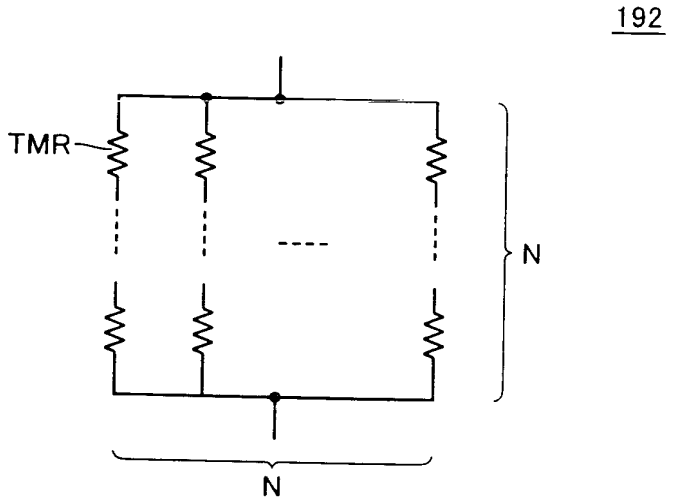

FIG.9

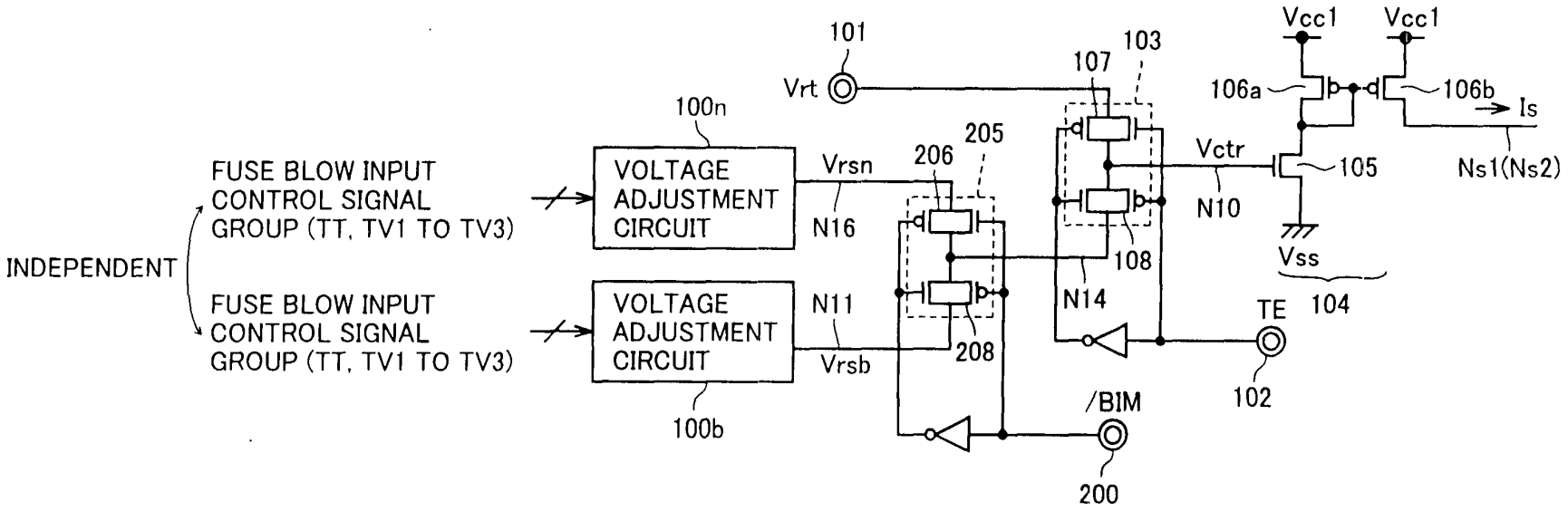
70 (71)
INDEPENDENT
FUSE BLOW INPUT CONTROL SIGNAL GROUP (TT, TV1 TO TV3)
FUSE BLOW INPUT CONTROL SIGNAL GROUP (TT, TV1 TO TV3)
VOLTAGE ADJUSTMENT CIRCUIT
VOLTAGE ADJUSTMENT CIRCUIT
100n
100b
101
Vrt
Vrsn
Vrsb
N16
N11
205
206
208
107
103
108
N14
N10
Vctr
Vcc1
Vcc1
106a
106b
105
Is
Ns1(Ns2)
Vss
104
TE
102
/BIM
200

FIG.10

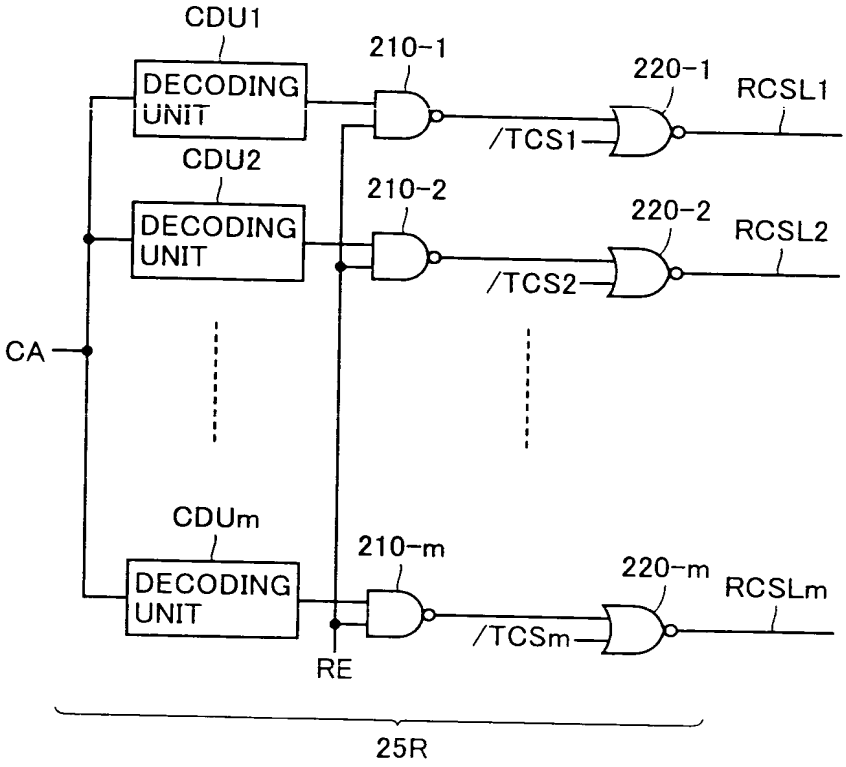
CDU1
DECODING UNIT
210-1
220-1
RCSL1
/TCS1
CDU2
DECODING UNIT
210-2
220-2
RCSL2
/TCS2
CA
CDUm
DECODING UNIT
210-m
220-m
RCSLm
/TCSm
RE
25R

FIG.11

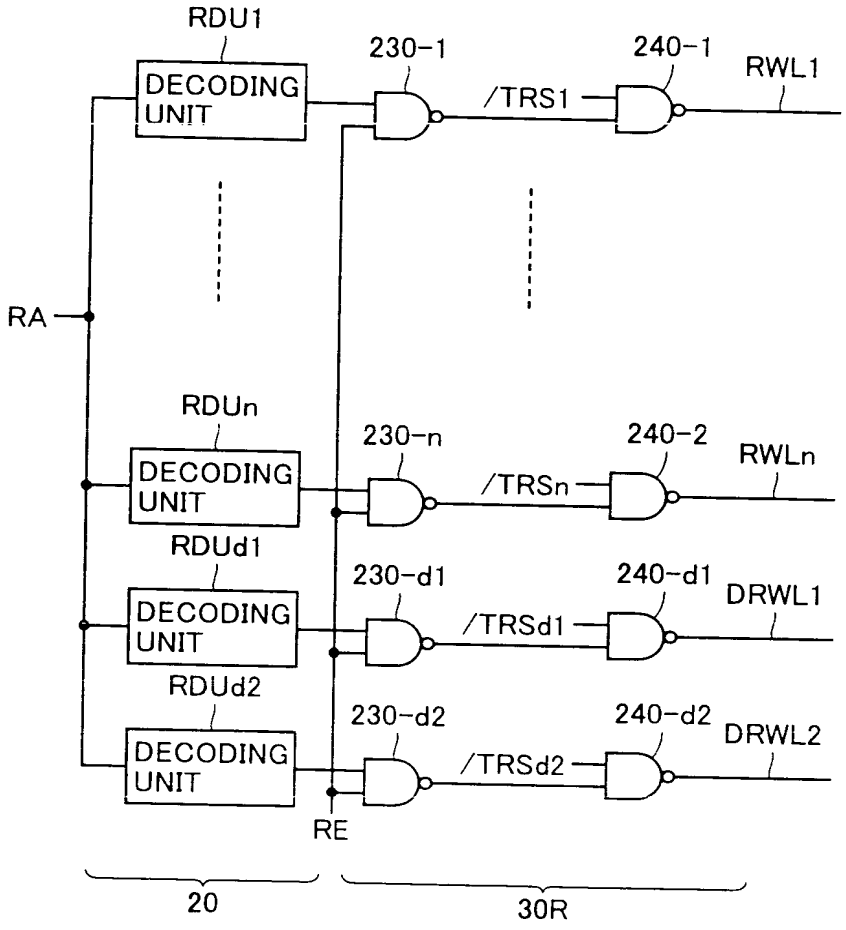
RDU1
DECODING UNIT
230-1
240-1
/TRS1
RWL1
RA
RDUn
DECODING UNIT
230-n
240-2
/TRSn
RWLn
RDUd1
DECODING UNIT
230-d1
240-d1
/TRSd1
DRWL1
RDUd2
DECODING UNIT
230-d2
240-d2
/TRSd2
DRWL2
RE
20
30R

FIG.12

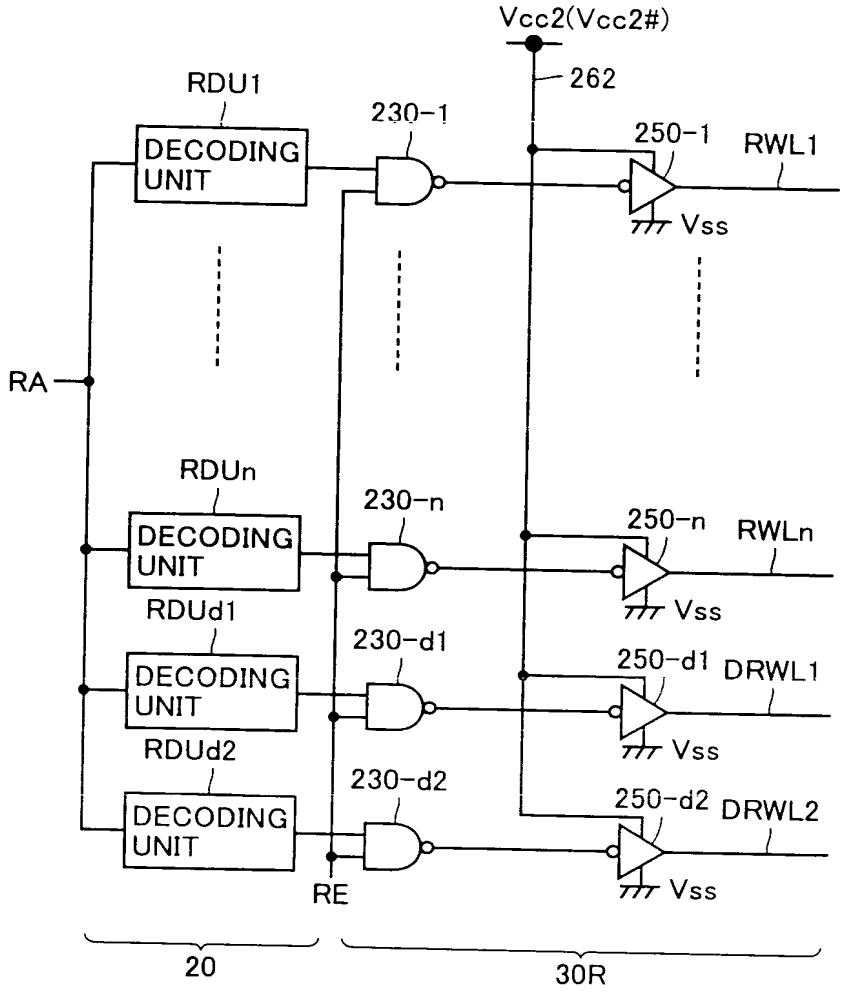
Vcc2(Vcc2#)
262
RDU1
DECODING UNIT
230-1
250-1
RWL1
Vss
RA
RDUn
DECODING UNIT
230-n
250-n
RWLn
Vss
RDUd1
DECODING UNIT
230-d1
250-d1
DRWL1
Vss
RDUd2
DECODING UNIT
230-d2
250-d2
DRWL2
Vss
RE
20
30R

FIG.13

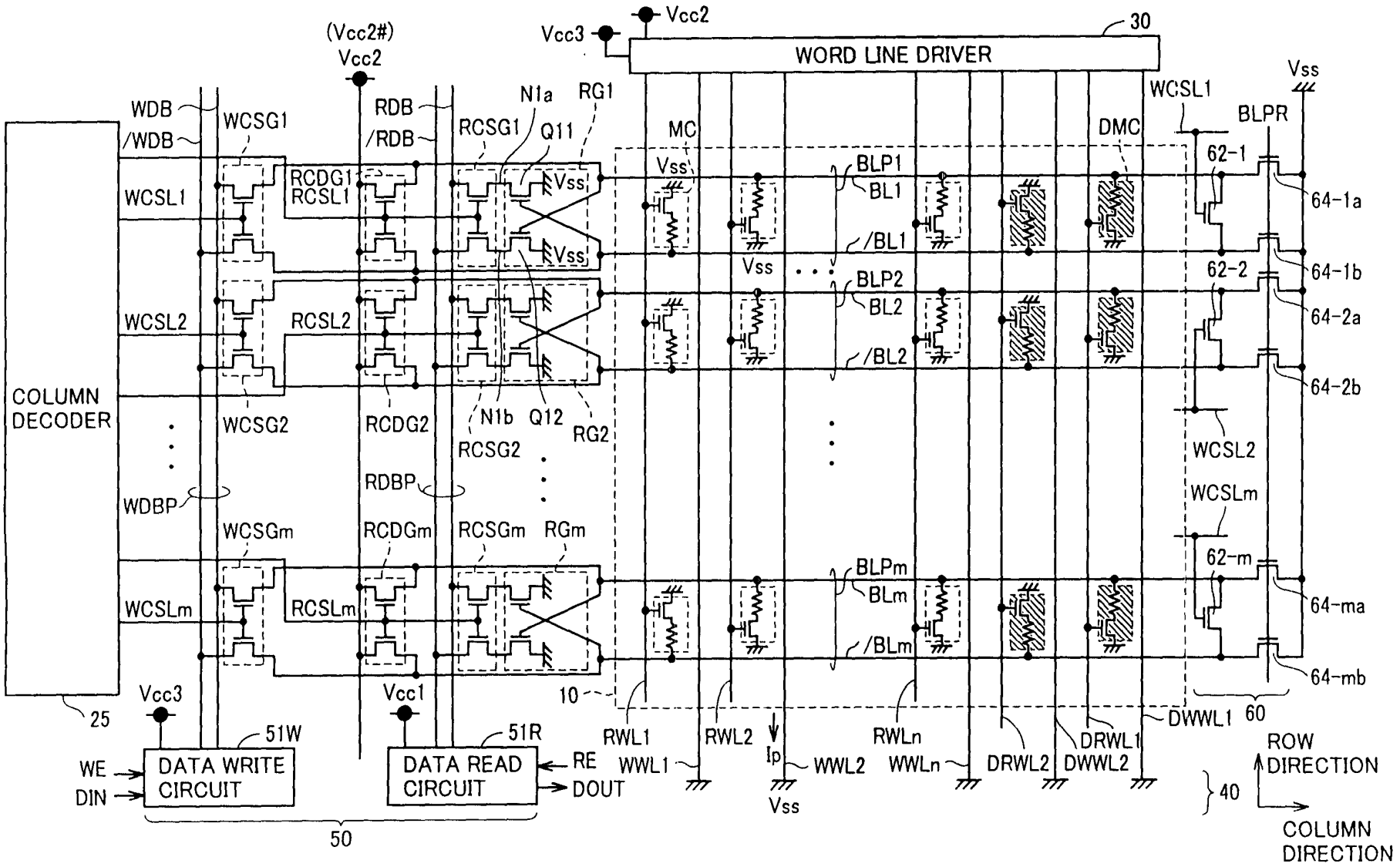
Vcc2
Vcc3
(Vcc2#)
Vcc2
30
WORD LINE DRIVER
Vss
WDB
/WDB
WCSG1
RDB
/RDB
RCSG1
N1a
RG1
Q11
MC
DMC
WCSL1
BLPR
62-1
64-1a
RCDG1
RCSL1
Vss
BLP1
BL1
/BL1
64-1b
62-2
64-2a
WCSL2
RCSL2
BLP2
BL2
/BL2
64-2b
COLUMN DECODER
WCSG2
RCDG2
N1b
Q12
RG2
RCSG2
WCSL2
WDBP
RDBP
WCSLm
WCSGm
RCDGm
RCSGm
RGm
62-m
BLPm
BLm
/BLm
64-ma
WCSLm
RCSLm
64-mb
Vcc3
Vcc1
10
25
51W
51R
RWL1
RWL2
Ip
RWLn
DRWL1
DWWL1
60
WE
DIN
DATA WRITE CIRCUIT
DATA READ CIRCUIT
RE
DOUT
WWL1
WWL2
WWLn
DRWL2
DWWL2
ROW DIRECTION
40
Vss
50
COLUMN DIRECTION

FIG.14

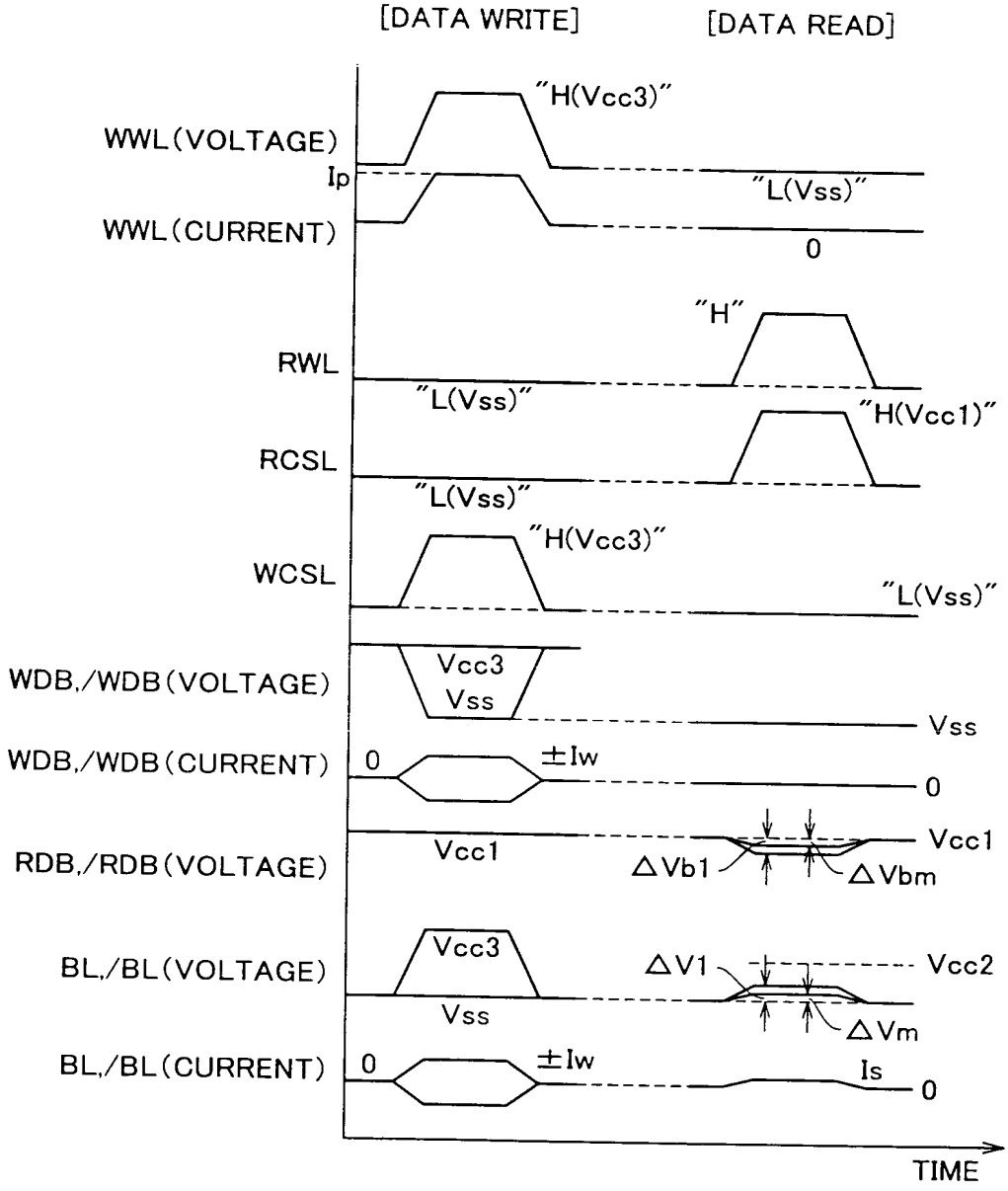
[DATA WRITE]
[DATA READ]
WWL(VOLTAGE)
"H(Vcc3)"
Ip
"L(Vss)"
WWL(CURRENT)
0
"H"
RWL
"L(Vss)"
"H(Vcc1)"
RCSL
"L(Vss)"
"H(Vcc3)"
WCSL
"L(Vss)"
WDB,/WDB(VOLTAGE)
Vcc3
Vss
Vss
WDB,/WDB(CURRENT)
0
±Iw
0
Vcc1
RDB,/RDB(VOLTAGE)
Vcc1
ΔVb1
ΔVbm
BL,/BL(VOLTAGE)
Vcc3
ΔV1
Vcc2
Vss
ΔVm
BL,/BL(CURRENT)
0
±Iw
Is
0
TIME

FIG.15

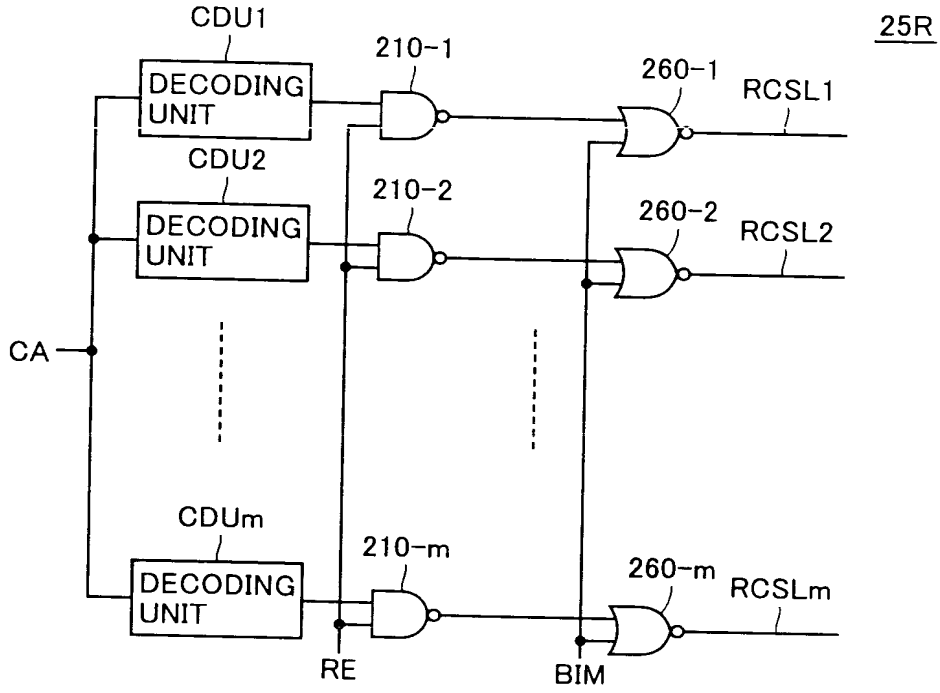
25R
CDU1
DECODING UNIT
210-1
260-1
RCSL1
CDU2
DECODING UNIT
210-2
260-2
RCSL2
CA
CDUm
DECODING UNIT
210-m
260-m
RCSLm
RE
BIM

FIG.16

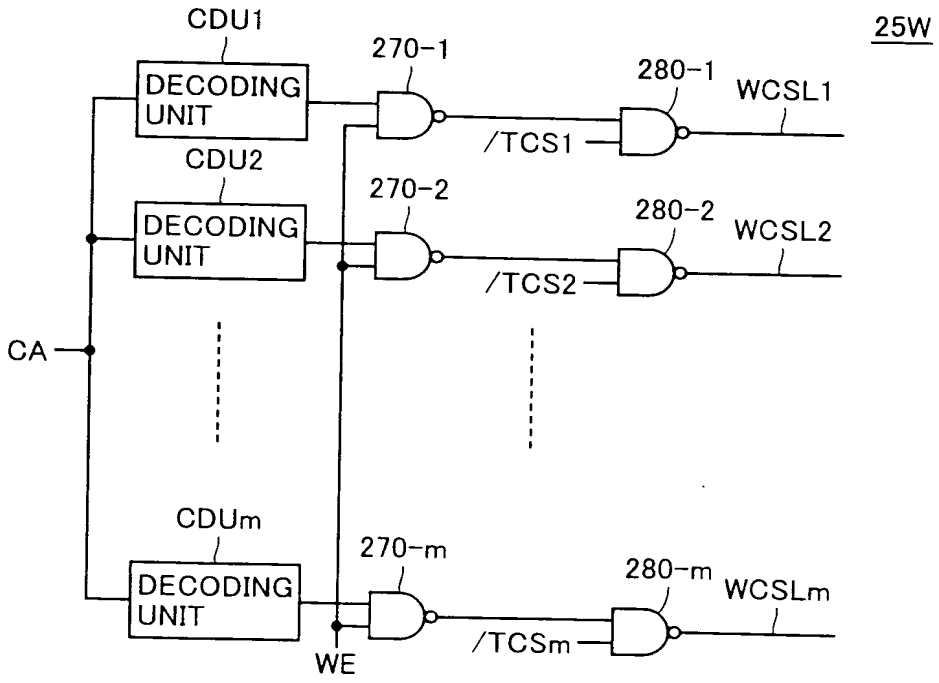
25W
CDU1
DECODING UNIT
270-1
280-1
WCSL1
/TCS1
CDU2
DECODING UNIT
270-2
280-2
WCSL2
/TCS2
CA
CDUm
DECODING UNIT
270-m
280-m
WCSLm
/TCSm
WE

FIG.17

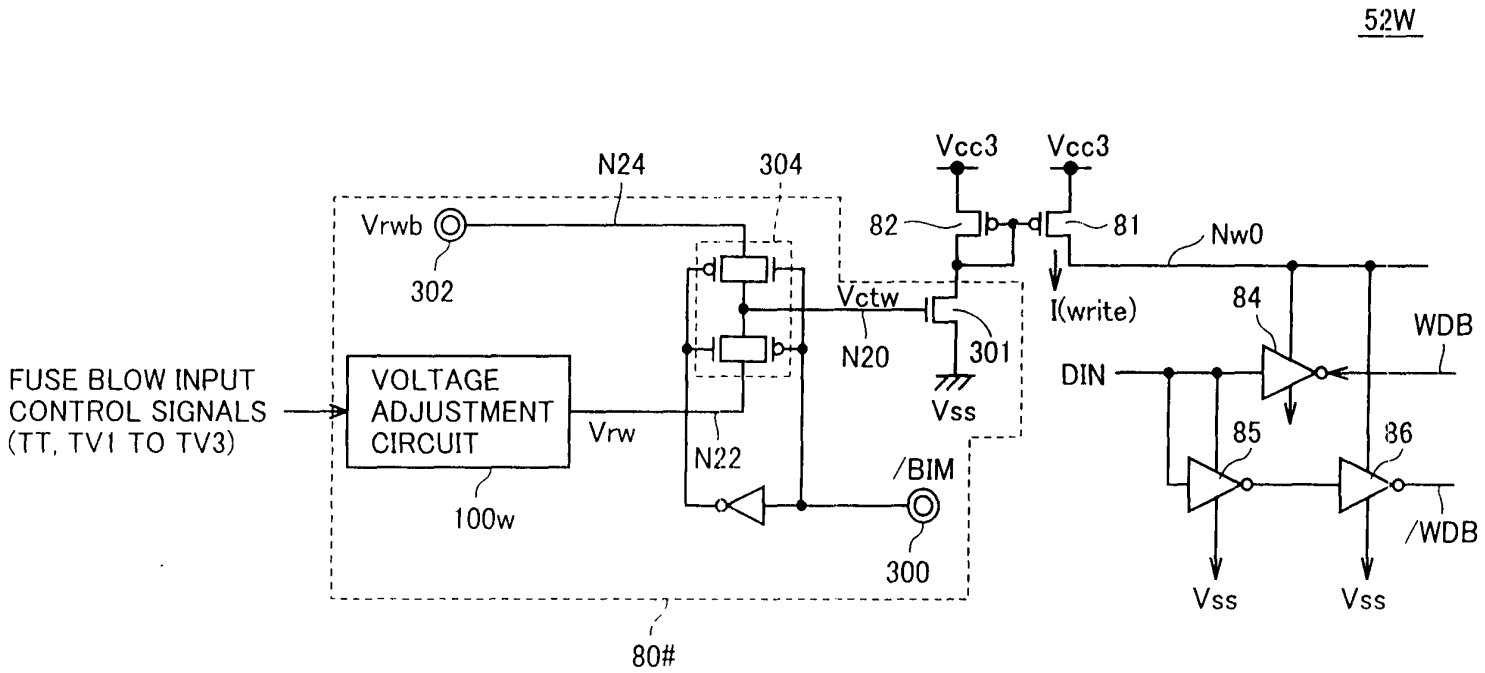
52W
N24
304
Vcc3
Vcc3
Vrwb
302
82
81
Nw0
Vctw
I(write)
84
WDB
FUSE BLOW INPUT
CONTROL SIGNALS
(TT, TV1 TO TV3)
VOLTAGE
ADJUSTMENT
CIRCUIT
100w
Vrw
N22
N20
301
Vss
DIN
85
86
/BIM
300
/WDB
Vss
Vss
80#

FIG.18

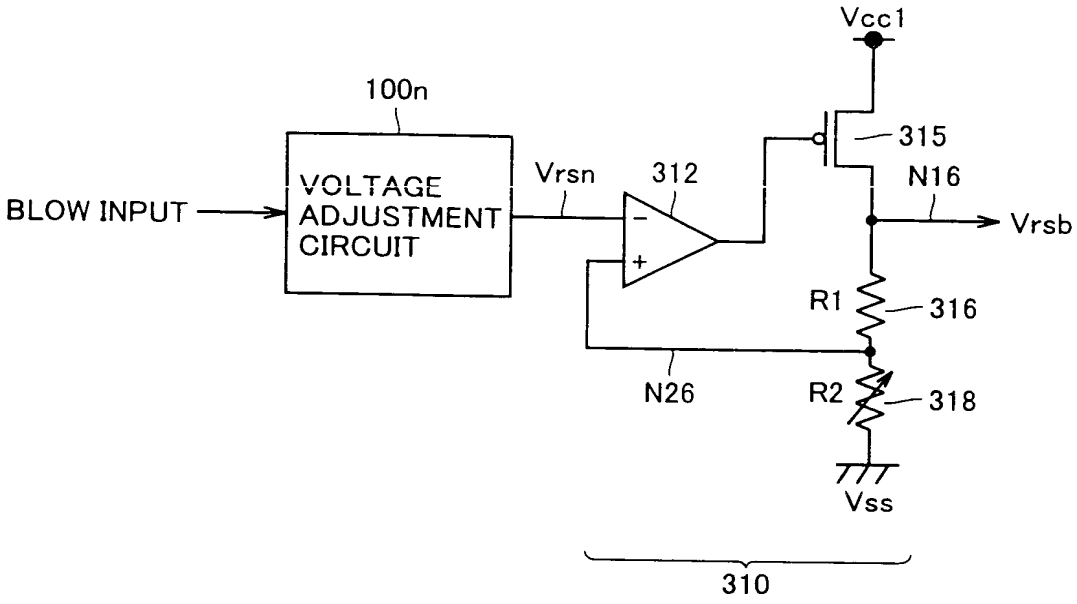
Vcc1
100n
315
VOLTAGE ADJUSTMENT CIRCUIT
Vrsn
312
N16
BLOW INPUT
Vrsb
R1
316
N26
R2
318
Vss
310

FIG.19

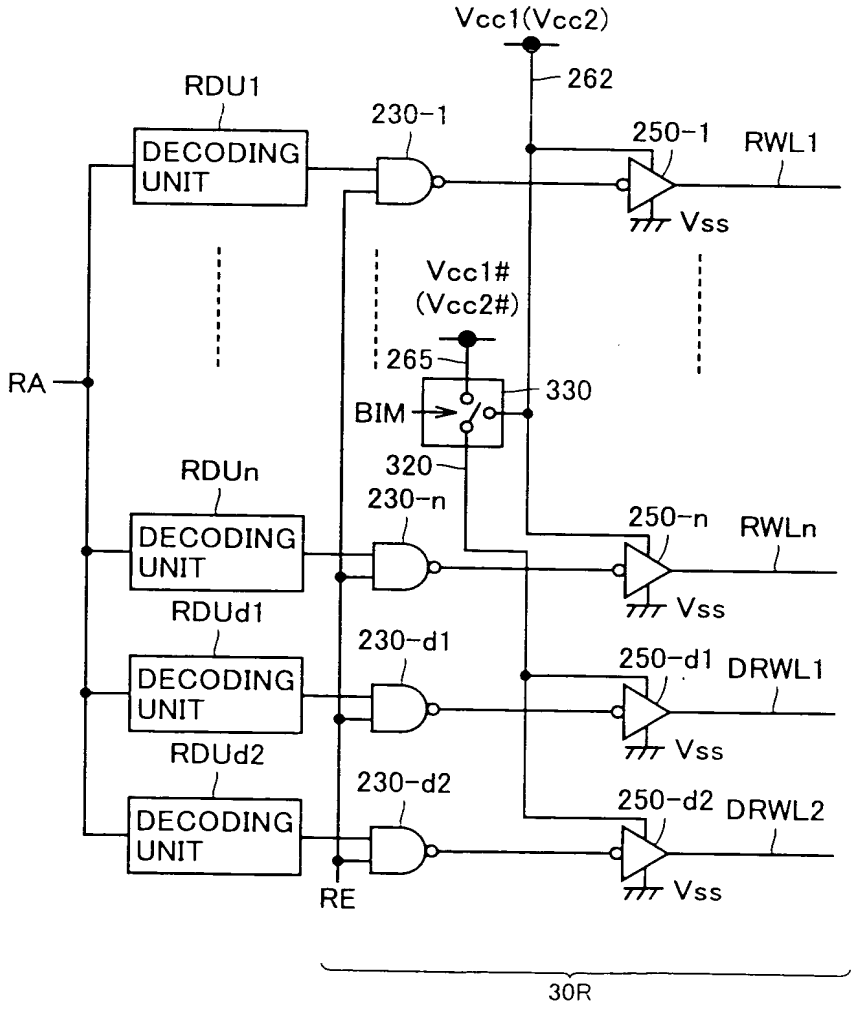
Vcc1(Vcc2)
262
RDU1
230-1
250-1
RWL1
DECODING UNIT
Vss
Vcc1#
(Vcc2#)
265
RA
330
BIM
320
RDUn
230-n
250-n
RWLn
DECODING UNIT
Vss
RDUd1
230-d1
250-d1
DRWL1
DECODING UNIT
Vss
RDUd2
230-d2
250-d2
DRWL2
DECODING UNIT
Vss
RE
30R

FIG.20

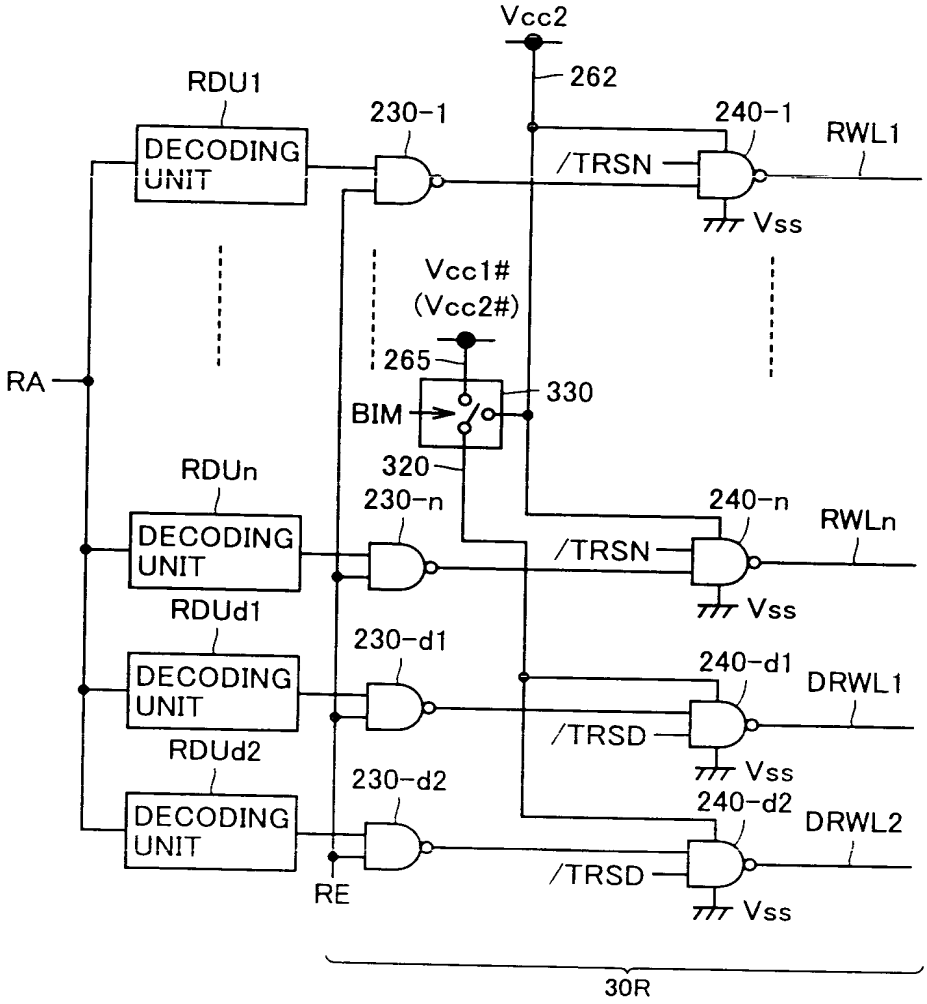
Vcc2
262
RDU1
230-1
240-1
RWL1
DECODING UNIT
/TRSN
Vss
Vcc1#
(Vcc2#)
265
330
BIM
320
RA
RDUn
230-n
240-n
RWLn
DECODING UNIT
/TRSN
Vss
RDUd1
230-d1
240-d1
DRWL1
DECODING UNIT
/TRSD
Vss
RDUd2
230-d2
240-d2
DRWL2
DECODING UNIT
/TRSD
Vss
RE
30R

FIG.21

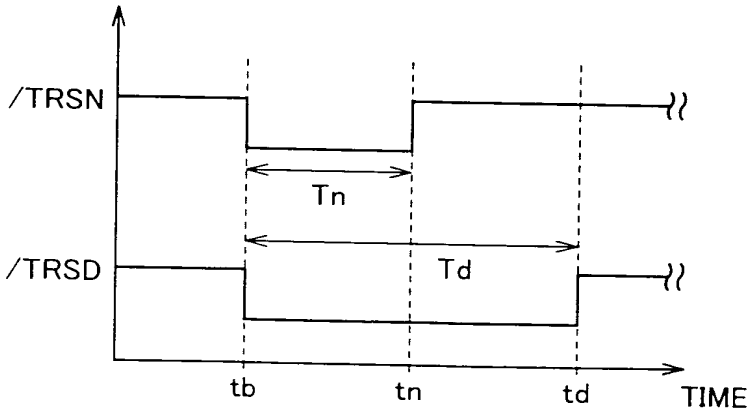
/TRSN
Tn
/TRSD
Td
tb
tn
td
TIME

FIG.22 PRIOR ART

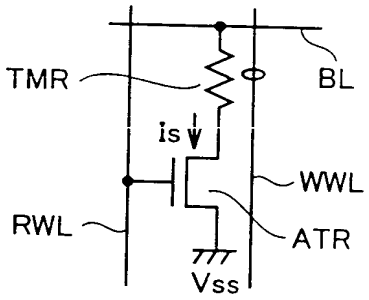

FIG.23 PRIOR ART

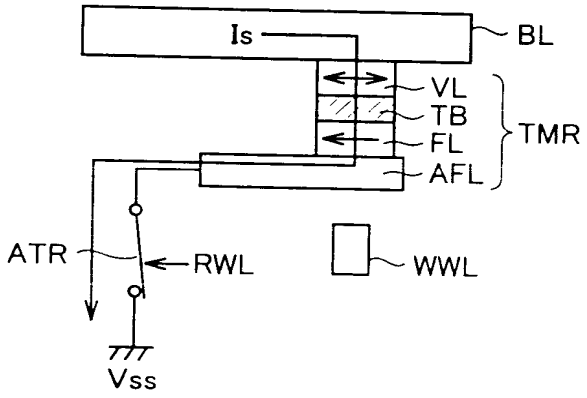

FIG.24 PRIOR ART

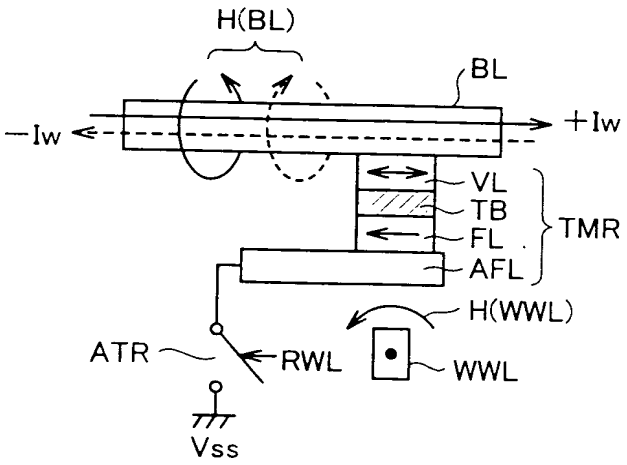

FIG.25 PRIOR ART